FIG. 1

CONCEPTUAL DIAGRAM ILLUSTRATING ERASE OPERATION OF NON-VOLATILE SEMICONDUCTOR MEMORY CELL

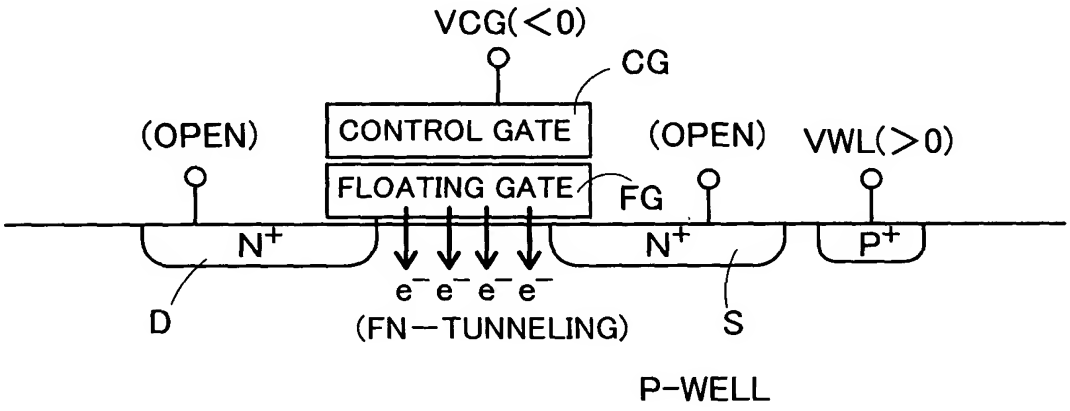


FIG. 2

CONCEPTUAL DIAGRAM ILLUSTRATING WRITE OPERATION OF NON-VOLATILE SEMICONDUCTOR MEMORY CELL

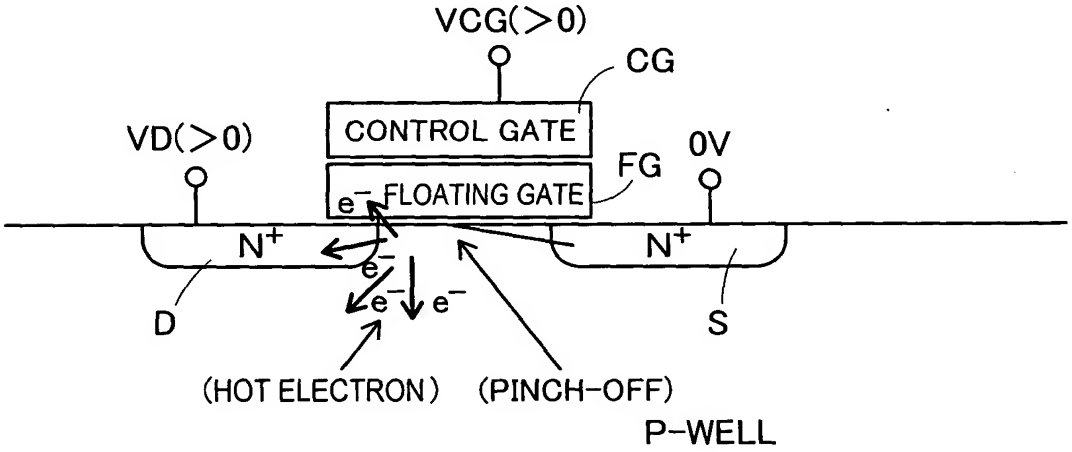
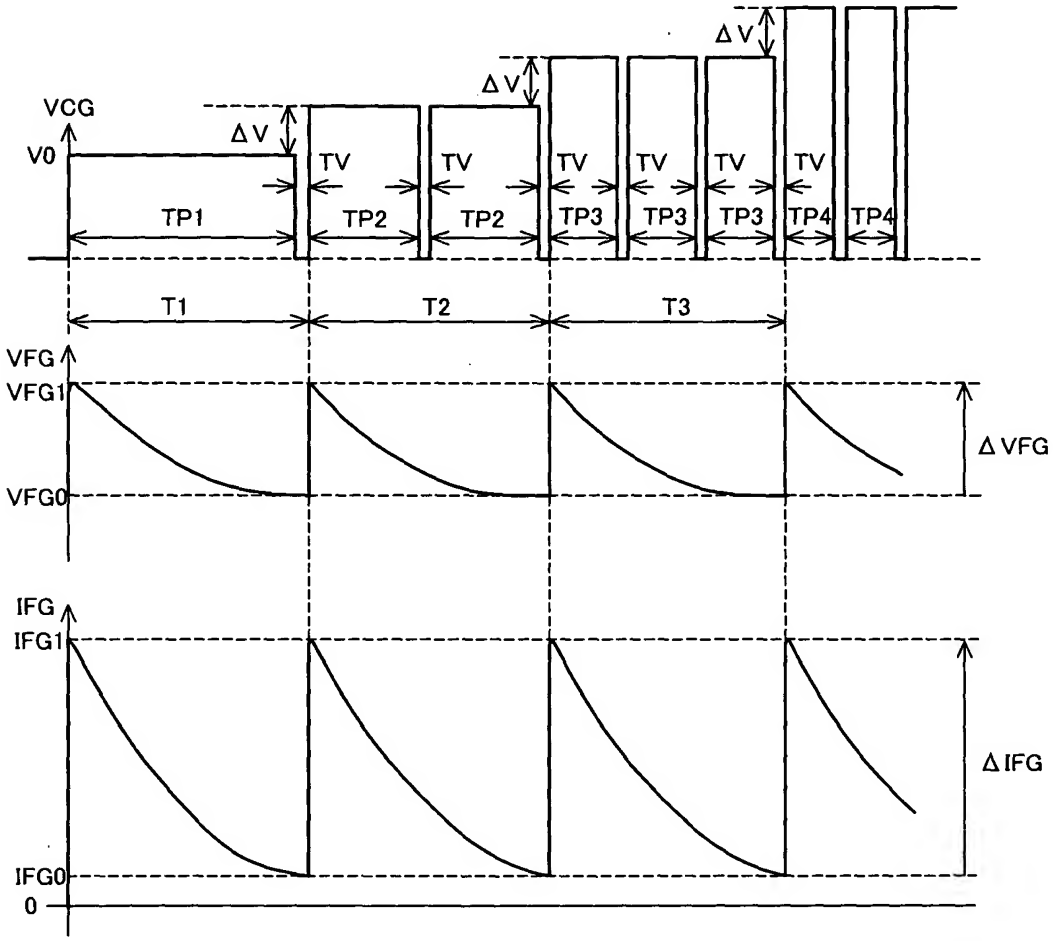


FIG. 3

WAVEFORM DIAGRAM DIRECTED TO FIRST EMBODIMENT



Title: CONTROL METHOD OF NON-VOLATILE SEMICONDUCTOR MEMORY CELL AND NON-VOLATILE SEMICONDUCTOR MEMORY DEVICE
Inventor: Shozo KAWABATA
Appln. No. : Unknown
Docket No.: 024016-00069

FIG. 4

WAVEFORM DIAGRAM DIRECTED TO VARIANT OF FIRST EMBODIMENT

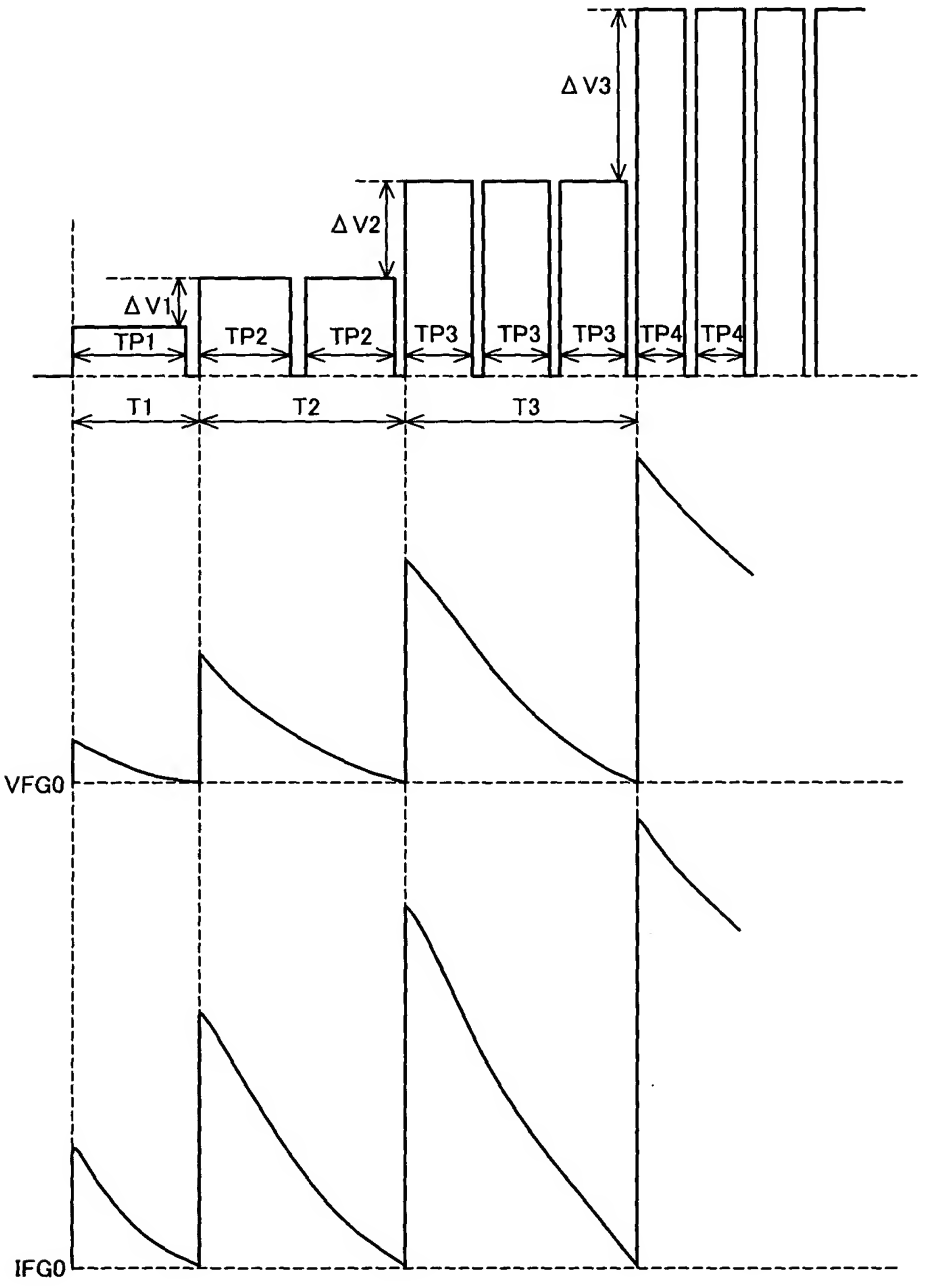
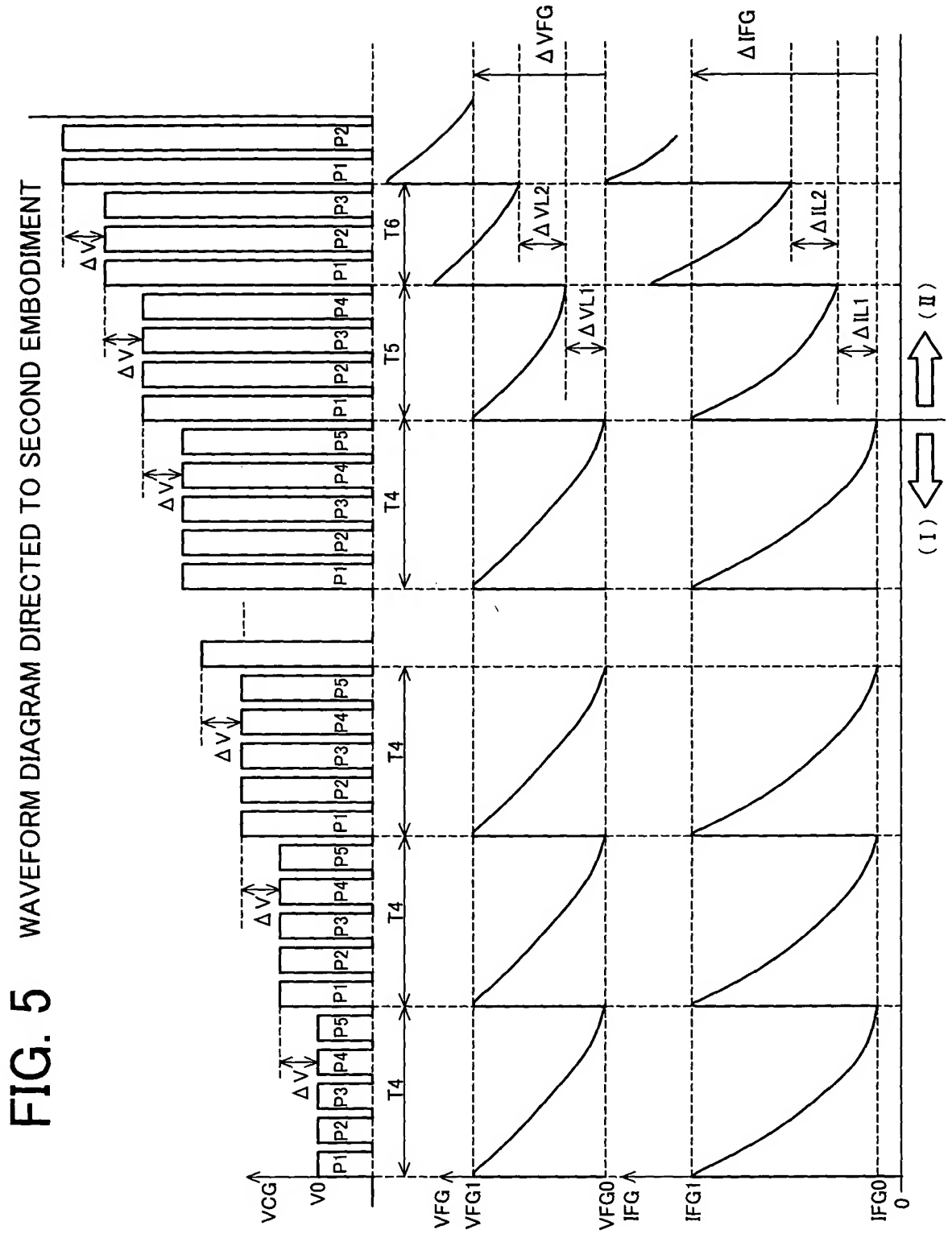


FIG. 5 WAVEFORM DIAGRAM DIRECTED TO SECOND EMBODIMENT



5

FIG. 6

WAVEFORM DIAGRAM DIRECTED TO THIRD EMBODIMENT

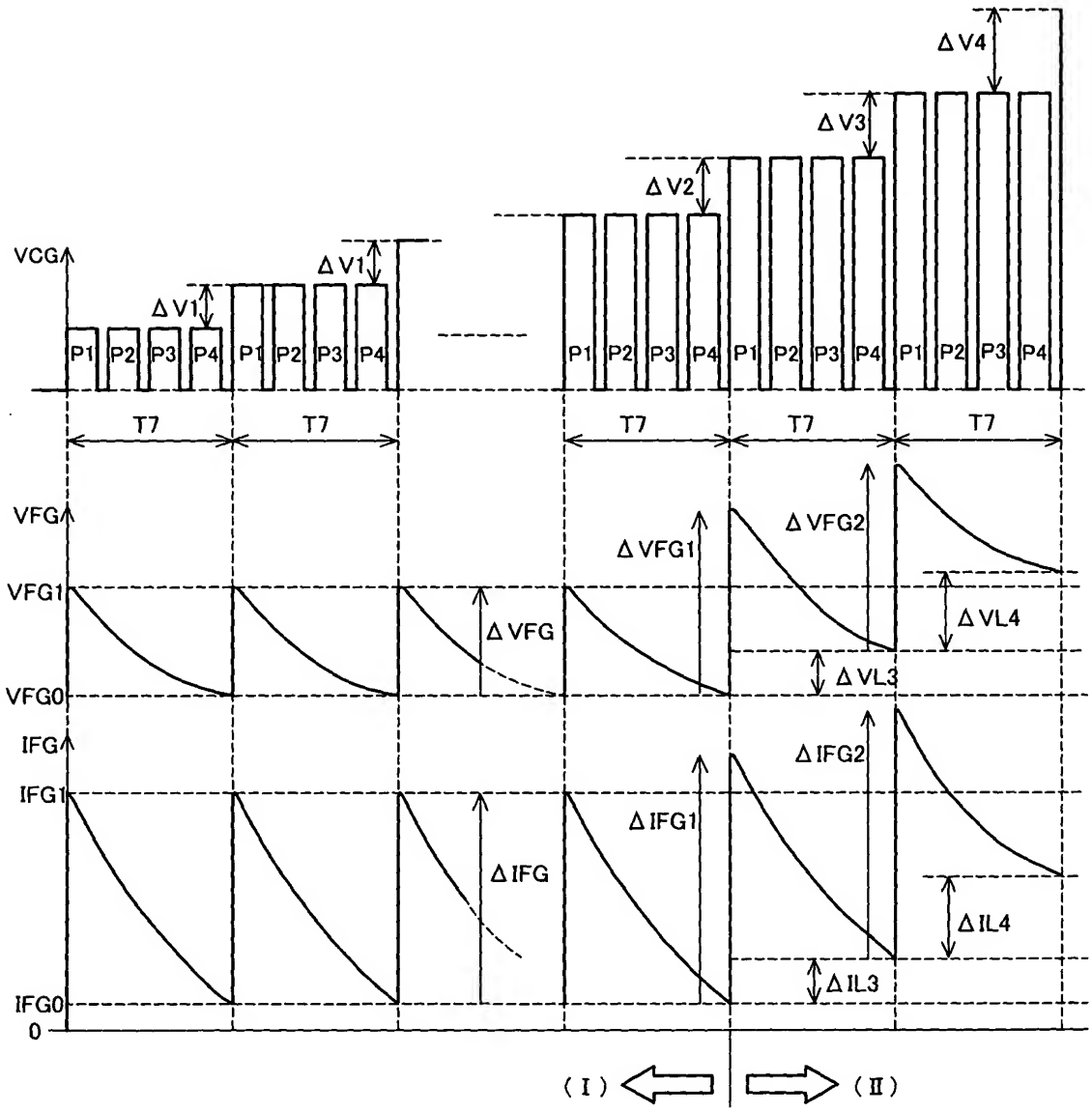


FIG. 7 CIRCUIT BLOCK DIAGRAM OF NON-VOLATILE SEMICONDUCTOR MEMORY DEVICE DIRECTED TO FOURTH EMBODIMENT

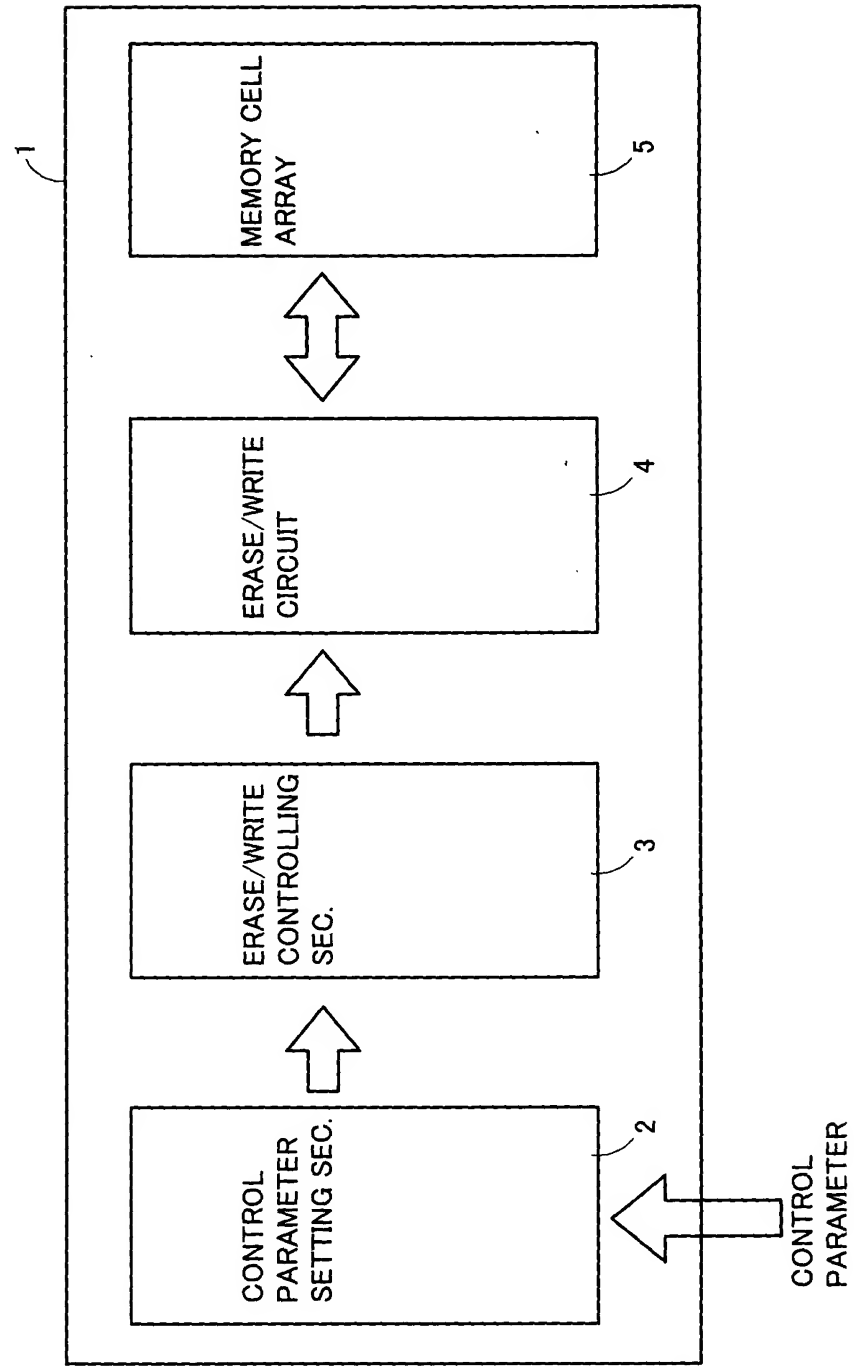


FIG. 8 PRIOR ART

WAVEFORM DIAGRAM DIRECTED TO RELATED ART